ABSTRACT:

A FIFO-register (10) according to the invention comprises a sequence of register cells (10.1,...,10.m), which register cells have a data section (40) and a status section (30). Data (Din) provided at an input (20) is shifted via the data sections (40) in the register cells to an output (50). The status section (30) of each cell indicates whether the data section (40) of that cell contains valid data. The status section of a cell comprises a control unit (37) coupled to a status input (32), to a status output (33) and to a clock input (31), and generates an output clock signal (Cl_i), which controls charge controlling elements (35, 36) coupled to the status input and the status output and controls the data section (40). The status output (33) of a status section (30) and the status input (32') of its successor (30') share a common capacitive node (33).

Figure 1.